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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,673	03/15/2004	Masashi Suzuki		8662

7590 07/12/2004

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EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,673	SUZUKI ET AL.	
	Examiner	Art Unit	
	Linh V Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09961250.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant' preliminary amendment filed on 05/14/04. Claims 15 – 37 are pending on this application.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 15 - 37 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 14 of U.S. Patent No. 6,731,167. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims 1 – 14 of the patent are disclosed every aspect of applicant's claimed invention except for not explicitly disclose the transistors for the bias control circuit are MOSFET. However bipolar and MOSFET transistors are well known and conventional in the art of transistors. It would have been obvious to one in the art at the time the invention to implement the transistors in the bias control circuit of the patent with either bipolar or MOSFET transistors to obtain the claimed invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 15 – 17, 21 – 31, and 34 are rejected under 35 U.S.C. 102(e) as being anticipate by Tsutsui et al. U.S. Patent No. 6,636,114.

6. Regarding to claim 15, Fig. 6 of Tsutsui discloses a high frequency power amplifier module, comprising : a high frequency power amplifier and a bias control circuit (Fig. 6), each of which is monolithically formed on a single semiconductor chip (Fig. 5) which is mounted on a module (Fig. 2 – 4) and which includes a first input (Pin-GSM900) terminal, a second input (Pin-GSM1800) terminal, a first output terminal (Pout-GSM900), and a second output (Pout-GSM1800) terminal, wherein said high frequency power amplifier includes: a first amplifying system (a) coupled to the first input terminal and to the first output terminal, and including a plurality of first bias terminals(Vgs1, Vgs2, Vgs3), and a plurality of amplifying stages (Tr1, Tr2, Tr3) which are sequentially cascaded between said first input terminal and said first output terminal and each of which is coupled to a corresponding one of the plurality of first bias terminals so as to receive a bias potential therefrom, wherein each of said amplifying

stages includes a MOSFET (TRs) having a first conductivity type and a gate coupled to the corresponding first bias terminal, and a second amplifying system (b) coupled to the second input terminal and to the second output terminal, and including a plurality of second bias terminals (Vgs4 ,Vgs5, Vgs6), and a plurality of amplifying stages (Tr10, Tr11, Tr12) which are sequentially cascaded between said second input terminal and said second output terminal and each of which is coupled to a corresponding one of the plurality of second bias terminals so as to receive a bias potential therefrom, wherein each of said amplifying stages includes a MOSFET having the first conductivity type and a gate coupled to the corresponding second bias terminal, wherein said bias control circuit includes a first MOSFET (Tr4, Tr13) of the first conductivity type and a second MOSFET (Tr5, Tr6, Tr14, Tr15)) of a second conductivity type and is coupled to the plurality of first bias terminals (Vgs1, Vgs4) and to the plurality of second bias terminals (Vgs2, Vgs3, Vgs5, Vgs6).

Regarding to claim 16, wherein said high frequency amplifier module has a first control terminal (Vapc-GSM900) and a second control terminal (Vpac-GSM1800), each of which are coupled to said bias control circuit, wherein said bias control circuit is arranged to receive a first control signal from said first control terminal, and to provide a bias voltage in accordance with the first control signal to said first amplifying system, and wherein said bias control circuit is arranged to receive a second control signal from second control terminal, and to provide a bias voltage in accordance with the second control signal to said second amplifying system.

Regarding to claim 17, wherein the second MOSFET (Tr2) of the second conductivity type is coupled with the first MOSFET (Tr1) of the first conductivity type in series, the second MOSFET coupled with a third MOSFET (Tr5) of the second conductivity type in parallel with their respective gate terminals connected to each other, and the gate terminal and drain terminal of the third MOSFET are connected to each other.

Regarding to claim 29, wherein each of said cascaded amplifying stages in said first amplifying system and said second amplifying system includes a control terminal (Gate input of MOSFET) and an output terminal, wherein said control terminals and said output terminals in each respective stage are alternatively provided in the same direction.

Regarding to claim 30, wherein said cascaded amplifying stages of said first amplifying system include first and second amplifying stages, each of said first and second amplifying stages including a control terminal (Gate input of MOSFET) and an output terminal, wherein the control terminal of said second amplifying stage of said first amplifying system and a wire connected to the output terminal of said second amplifying stage of said first amplifying system extend in directions crossing each other (Fig. 5).

Regarding to claim 31, wherein the wire that is connected to the control terminal of said second amplifying stage and the wire connected to the first terminal of said second amplifying stage extend in directions orthogonal to each other (Fig. 5).

Regarding to claim 34, a wireless communication apparatus comprising a high frequency power amplifier module to claim 15 (Col. 1 lines 1 – 5).

Regarding to claims 21 - 26, Fig. 5 of Tsutsui et al. as applied to claims 15 – 17 above, disclosed every aspect of applicant's claimed invention.

Regarding to claims 27 and 28, Fig. 5 of Tsutsui et al. as applied to claims 15 – 17 above, disclosed every aspect of applicant's claimed invention.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

LVN

06/29/04

Michael J. Tokar

Michael Tokar
Supervisory Patent Examiner
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